CFM8133

Dual H-Bridge Motor Driver

1 Description

The CFM8133 device provides a dual bridge motor driver solution for toys, printers, and other mechatronic applications.

The device has two H-bridge drivers, and can drive two DC brush motors, a bipolar stepper motor, solenoids, or other inductive loads.

The output driver block of each H-bridge consists of N-channel power MOSFETs configured as an H- bridge to drive the motor windings. Each H-bridge includes circuitry to regulate or limit the winding current.

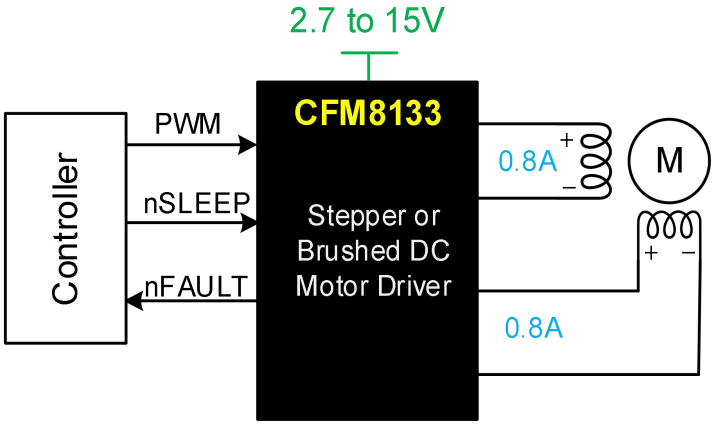
Internal shutdown functions with a fault output pin are provided for overcurrent protection, short-circuit protection, and overtemperature. A low-power sleep mode is also provided.

The CFM8133 is packaged in a 16-pin HTSSOP package with Power PAD.

2 Applications

- Battery-Powered Toys
- POS Printers
- Video Security Cameras
- Office Automation Machines
- Gaming Machines
- Robotics

Simplified Schematic



3 Features

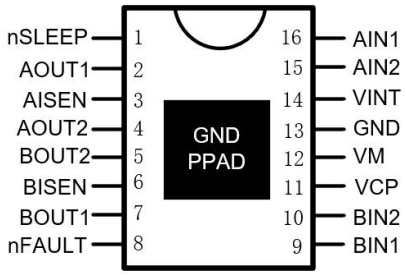
- Dual H-Bridge Current Control Motor Driver
  - Can Drive Two DC Motors or One Stepper Motor
  - Low MOSFET On Resistance: HS + LS = 800 mΩ
- Output Current (at VM = 5 V, 25°C)
  - 0.8A RMS, 1.2A Peak per H-Bridge in PWP Package Option
- Outputs can be in Parallel for
  - 1.6A RMS, 2.4A Peak (PWP)
- Wide Power Supply Voltage Range: 2.7 to 15 V
- PWM Winding Current Regulation and Current Limiting
- Thermally Enhanced Surface-Mount Packages

4 Device Information

PARTNUMBER	PACKAGE	BODY SIZE (NOM)
CFM8133T	HTSSOP16	5.00mm x 4.40mm

5 Pin Configuration and Functions

Top View



Pin Functions

HTSSOP	NAME	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
1	nSLEEP	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode and reset all internal logic. Internal pulldown.
2	AOUT1	Bridge A output 1	Connect to motor winding A.
3	AISEN	Bridge A ground / I_{SENSE}	Connect to current sense resistor for bridge A, or GND if current control not needed.
4	AOUT2	Bridge A output 2	Connect to motor winding A.
5	BOUT2	Bridge B output 2	Connect to motor winding B.
6	BISEN	Bridge B ground / I_{SENSE}	Connect to current sense resistor for bridge B, or GND if current control not needed.
7	BOUT1	Bridge B output 1	Connect to motor winding B.
8	nFAULT	Fault output	Logic low when in fault condition (overtemperature, overcurrent)
9	BIN1	Bridge B input 1	Logic input controls state of BOUT1. Internal pulldown.
10	BIN2	Bridge B input 2	Logic input controls state of BOUT2. Internal pulldown.
11	VCP	High-side gate drive voltage	Connect a10nFto 100nF, 16V (minimum) X7R ceramic capacitor to VM.
12	VM	Device power supply	Connect to motor supply. A 10μF (minimum) ceramic bypass capacitor to GND is recommended.
13	GND	Device ground.HTSSOP package has PowerPAD	Both the GND pin and device PowerPAD must be connected to ground.
14	VINT	Internal supply bypass	Bypass to GND with 2.2μF, 6.3V capacitor.
15	AIN2	Bridge A input 2	Logic input controls state of AOUT2. Internal pulldown.
16	AIN1	Bridge A input 1	Logic input controls state of AOUT1. Internal pulldown.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VM	Power supply voltage	-0.3	16	V
	Digital input pin voltage	-0.5	7	V
	xISEN pin voltage	-0.3	0.5	V
	Peak motor drive output current	Internally limited		A
T_J	Operating junction temperature	-40	125	°C
T_{stg}	Storage temperature	-60	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stressratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	HBM	±2000	V
		CDM	±1000	

6.3 Thermal Resistance

Package	$R_{\theta JA}$	UNIT
HTSSOP16	40.5	°C/W
WQFN16	37.2	°C/W

6.4 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	2.7	--	14	V
V_{DIGIN}	Digital input pin voltage range	-0.3	--	5.5	V
I_{OUT}	RTY package continuous RMS or DC output current per bridge(2)	--	--	0.8	A

(1) $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) VM = 5 V, power dissipation and thermal limits must be observed.

6.5 Electrical Characteristics

TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	VM = 5 V, xIN1 = 0 V, xIN2 = 0 V	--	0.9	1.5	mA
I_{VMQ}	VM sleep mode supply current	VM = 5 V	--	--	1	μA
V_{UVLO}	VM undervoltage lockout voltage	VM falling	--	--	2.6	V
V_{HYS}	VM undervoltage lockout hysteresis		--	90	--	mV
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage	nSLEEP	--	--	0.5	V
		All other pins	--	--	0.7	
V_{IH}	Input high voltage	nSLEEP	--	2.5	--	V
		All other pins	--	2	--	
V_{HYS}	Input hysteresis		--	0.4	--	V
R_{IN}	Input pulldown resistance	nSLEEP	--	254	--	kΩ
		All except nSLEEP	--	165	--	
I_{IL}	Input low current	VIN = 0	--	--	1	μA
I_{IH}	Input high current	VIN = 3.3 V, nSLEEP	--	13	26	μA
		VIN = 3.3 V, all except nSLEEP	--	20	40	
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA	--	--	0.5	V
I_{LK}	Output high leakage current	V_O = 5 V	--	--	1	μA
H-BRIDGE FETs						
$R_{DS(ON)}$	HS FET on resistance	VM = 5 V, I_O = 500 mA, T_J = 25°C	--	400	--	mΩ
		VM = 2.7 V, I_O = 500 mA, T_J = 25°C	--	500	--	
	LS FET on resistance	VM = 5 V, I_O = 500 mA, T_J = 25°C	--	400	--	
		VM = 2.7 V, I_O = 500 mA, T_J = 25°C	--	500	--	
I_{OFF}	Off-state leakage current	VM = 5 V, T_J = 25°C, V_{OUT} = 0 V	-1	--	1	μA
MOTOR DRIVER						
f_{PWM}	Current control PWM frequency	Internal PWM frequency	--	35	--	kHz
t_{RISE}	Rise time	VM = 5 V, 16 Ω to GND, 10% to 90% VM	--	40	--	ns
t_{FALL}	Fall time	VM = 5 V, 16 Ω to GND, 10% to 90% VM	--	30	--	ns
t_{PD}	Propagation delay INx to OUTx	VM = 5 V	--	120	--	ns
DT	Dead time (1)	VM = 5 V	--	300	--	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		0.9	1.6	--	A
t_{DEG}	OCP Deglitch time		--	4	--	μs

t_{OCP}	Overcurrent protection period		--	1.6	--	ms
t_{TSD}	Thermal shutdown temperature	Die temperature	150	165	180	°C
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{OFF}	Constant Off Time		--	25	--	μs
t_{BLANK}	Current sense blanking time		--	3	--	μs
SLEEP MODE						
t_{WAKE}	Start-up time	nSLEEP inactive high to H-bridge on	--	1	--	ms

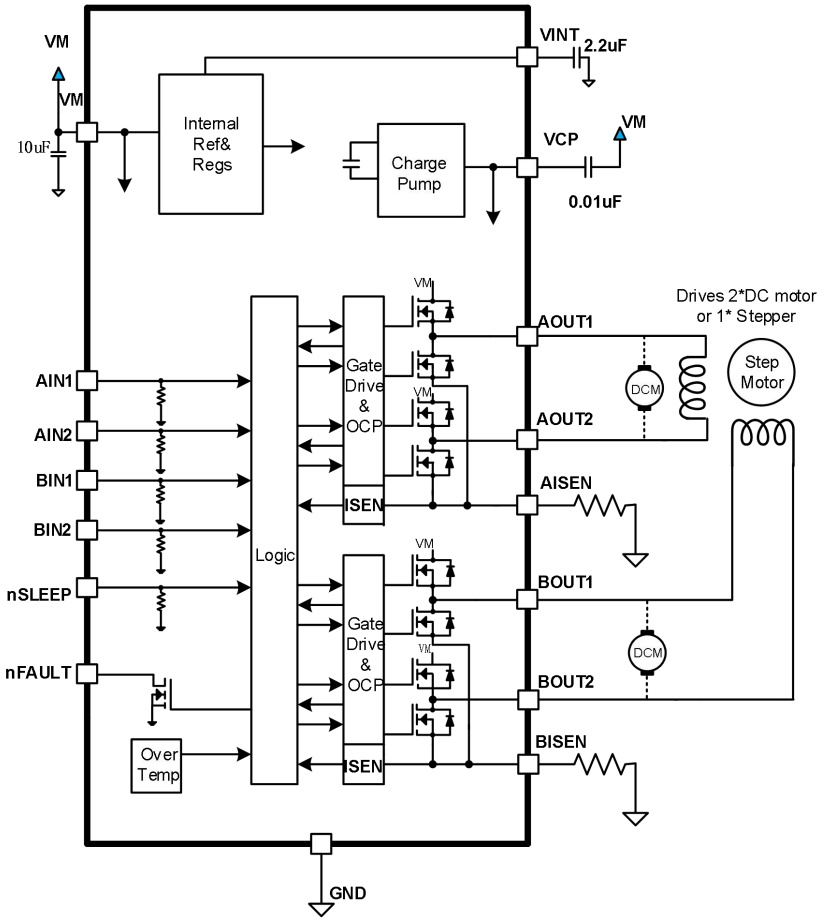
(1) Internal dead time. External implementation is not necessary.

7 Detailed Description

7.1 Overview

The CFM8133 device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two NMOS H-bridges and current regulation circuitry. The CFM8133 can be powered with a supply voltage from 2.7 to 15 V and can provide an output current up to 0.8A RMS. A simple PWM interface allows easy interfacing to the controller circuit. The current regulation is a fixed frequency PWM slow decay. The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

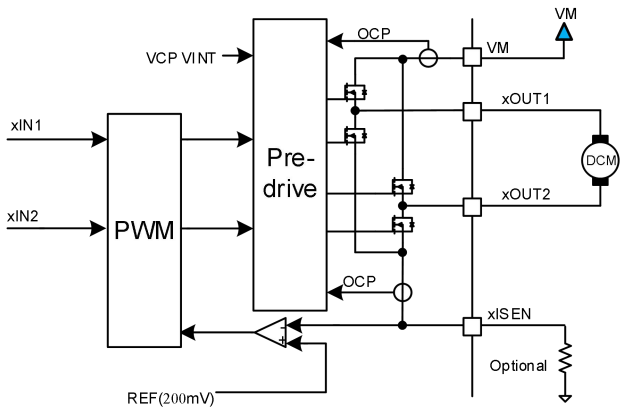
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Motor Drivers

CFM8133 contains two identical H-bridge motor drivers with current-control PWM circuitry. 1 shows a block diagram of the circuitry.



1. Motor Control Circuitry

7.3.2 Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs. 表 1 shows the logic.

表 1. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/slow decay

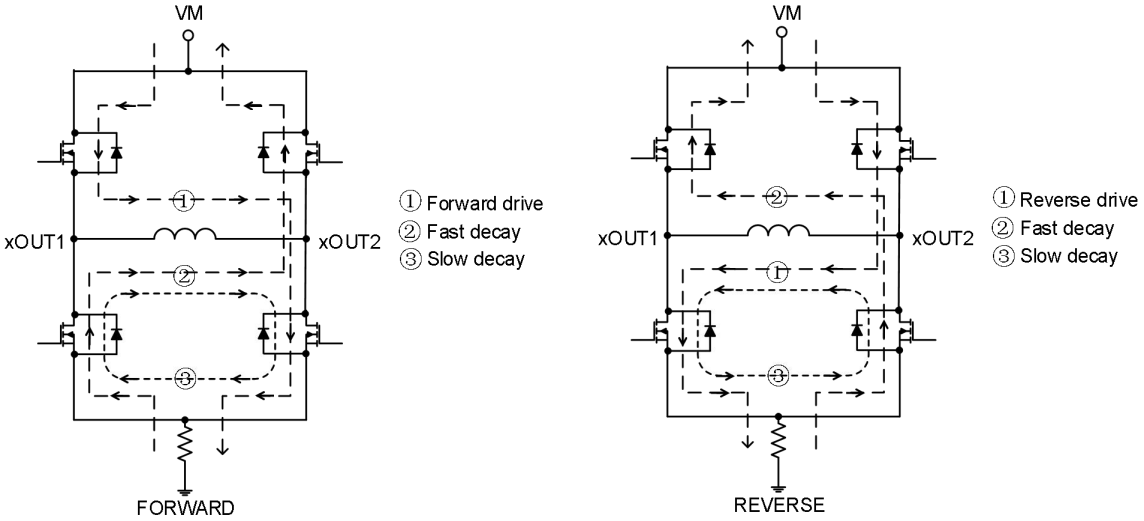
The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states: fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to one xIN pin while the other is held low; to use slow decay, one xIN pin is held high.

表 2. PWM Control of Motor Speed

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

2. shows the current paths in different drive and decay modes.



2. Drive and Decay Modes

7.3.3 Current Control

The current through the motor windings may be limited, or controlled, by a fixed-frequency PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.
When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Immediately after the current is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3μs. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.
The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage is fixed at 200 mV.
The chopping current is calculated in 公式 1.

$$I_{CHOP=}\frac{200mV}{R_{ISENSE}}$$

Example: If a 1Ω sense resistor is used, the chopping current will be 200 mV/1 Ω = 200 mA.

Once the chopping current threshold is reached, the H-bridge switches to slow decay mode. Winding current is recirculated by enabling both of the low-side FETs in the bridge. This state is held until the beginning of the next fixed-frequency PWM cycle.

If current control is not needed, the xISEN pins should be connected directly to ground.

7.3.4 nSLEEP Operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (up to 1 ms) needs to pass before the motor driver becomes fully operational.

7.3.5 Protection Circuits

The CFM8133 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.5.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will be re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Overcurrent protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xISEN resistor.

7.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

表 3. Device Protection

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	VM < 2.5 V	None	Disabled	Disabled	V_M > 2.7 V
Overcurrent (OCP)	I_{OUT} > I_{OCP}	FAULTn	Disabled	Operating	OCP
Thermal Shutdown (TSD)	T_J > T_{TSD}	FAULTn	Disabled	Operating	T_J < T_{TSD} – T_{HYS}

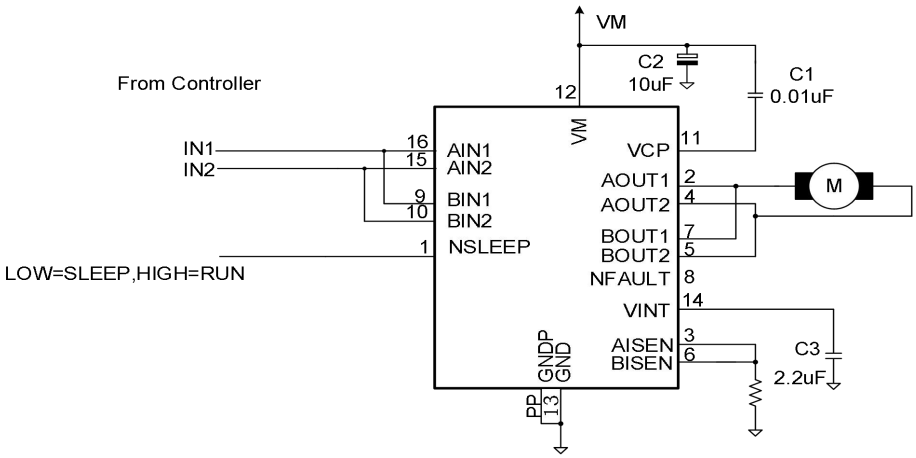
7.4 Device Functional Modes

The CFM8133 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled (Hi-Z). The CFM8133 is brought out of sleep mode automatically if nSLEEP is brought logic high. t_{WAKE} must elapse before the outputs change state after wakeup.

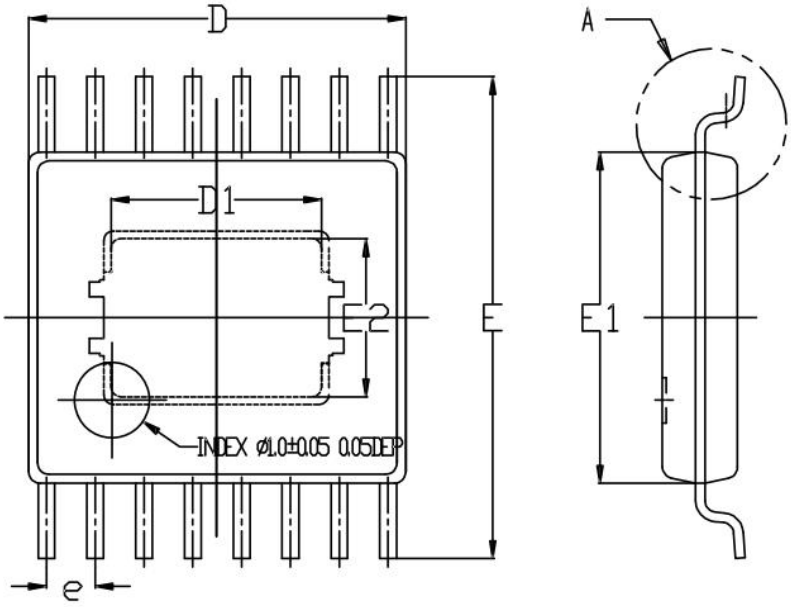
表 4. Modes of Operation

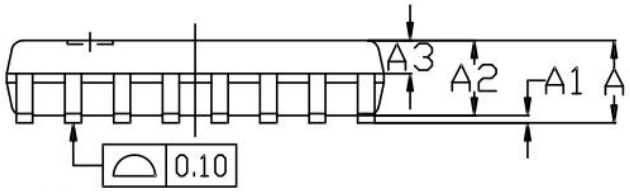
FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	nSLEEP pin high	Operating	Operating
Sleep mode	nSLEEP pin low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See 表 3

7.5 Typical Application



8 PACKAGE OUTLINE





NOTES:
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05	0.10	0.15
A2	0.965	1.000	1.035
A3	0.415	0.440	0.465
b	0.20		0.29
b1	0.19	0.22	0.25
c	0.13		0.18
c1	0.119	0.127	0.135
D	4.985	5.02	5.055
D1	2.70	2.80	2.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.00	2.10	2.20
L	0.45	0.60	0.75
e	0.65BSC		
L1	1.00REF		
L2	0.25BSC		

9 Ordering Information

Order Part No.	Package	QTY
CFM8133T	HTSSOP16, Pb-Free	3000/Reel